## CLAIMS

1. (Original) A multi-link receiving mechanism, comprising:

a first receiver coupled to receive a first data stream and a clock signal, said first data stream comprising a first plurality of data units, said first receiver delaying said clock signal by a first variable delay to derive a first reference signal, and generating a first plurality of latching control signals based upon said first reference signal to latch said first plurality of data units; and

A1

a second receiver coupled to receive a second data stream and said clock signal, said second data stream comprising a second plurality of data units, said second receiver delaying said clock signal by a second variable delay to derive a second reference signal, and generating a second plurality of latching control signals based upon said second reference signal to latch said second plurality of data units.

2. (Original) The receiving mechanism of claim 1, wherein said first data stream and said second data stream are not aligned with each other when received by said first receiver and second receiver, respectively.

3. (Original) The receiving mechanism of claim 2, wherein said clock signal is not necessarily aligned with either said first data stream or said second data stream.

4. (Original) The receiving mechanism of claim 3, wherein said first receiver adjusts said first variable delay based upon relative alignment between said first data stream and said clock signal.

5. (Currently amended) ~~The~~ A multi-link receiving mechanism ~~of claim 4,~~ comprising:

a first receiver coupled to receive a first data stream and a clock signal, said first data stream comprising a first plurality of data units, said first receiver delaying said clock signal by a first variable delay to derive a first reference signal, and generating a first plurality of latching control signals based upon said first reference signal to latch said first plurality of data units; and

a second receiver coupled to receive a second data stream and said clock signal, said second data stream comprising a second plurality of data units, said second receiver delaying said clock signal by a second variable delay to derive a second reference signal, and

generating a second plurality of latching control signals based upon said second reference signal to latch said second plurality of data units;

wherein said first data stream and said second data stream are not aligned with each other when received by said first receiver and second receiver, respectively;

wherein said clock signal is not necessarily aligned with either said first data stream or said second data stream;

wherein said first receiver adjusts said first variable delay based upon relative alignment between said first data stream and said clock signal; and

A1

wherein said second receiver adjusts said second variable delay based upon relative alignment between said second data stream and said clock signal.

6. (Original) The receiving mechanisms of claim 3, wherein said first variable delay and said second variable delay are different delays.

7. (Currently amended) ~~The~~ A multi-link receiving mechanism ~~of claim 6,~~ comprising:

a first receiver coupled to receive a first data stream and a clock signal, said first data stream comprising a first plurality of data units, said first receiver delaying said clock signal by a first variable delay to derive a first reference signal, and generating a first plurality of latching control signals based upon said first reference signal to latch said first plurality of data units; and

a second receiver coupled to receive a second data stream and said clock signal, said second data stream comprising a second plurality of data units, said second receiver delaying said clock signal by a second variable delay to derive a second reference signal, and generating a second plurality of latching control signals based upon said second reference signal to latch said second plurality of data units;

wherein said first data stream and said second data stream are not aligned with each other when received by said first receiver and second receiver, respectively;

wherein said clock signal is not necessarily aligned with either said first data stream or said second data stream;

wherein said first variable delay and said second variable delay are different delays; and

wherein each of said first plurality of data units occupies one data period;

wherein each of said second plurality of data units occupies one data period; and

wherein both said first variable delay and said second variable delay are greater than or equal to one data period.

8. (Original) The receiving mechanism of claim 3, wherein each of said first plurality of data units occupies one data period, and wherein said first reference signal coincides approximately with a midpoint of a data period corresponding to one of said first plurality of data units.

9. (Original) The receiving mechanism of claim 8, wherein each of said second plurality of data units occupies one data period, and wherein said second reference signal coincides approximately with a midpoint of a data period corresponding to one of said second plurality of data units.

A1

10. (Original) The receiving mechanism of claim 3, wherein each of said first plurality of data units occupies one data period, and wherein said first receiver generates no more than one of said first plurality of latching control signals per data period.

11. (Original) The receiving mechanism of claim 10, wherein each of said first plurality of latching control signals coincides approximately with a midpoint of a data period corresponding to one of said first plurality of data units.

12. (Original) The receiving mechanism of claim 11, wherein each of said second plurality of data units occupies one data period, and wherein said second receiver generates no more than one of said second plurality of latching control signals per data period.

13. (Original) The receiving mechanism of claim 12, wherein each of said second plurality of latching control signals coincides approximately with a midpoint of a data period corresponding to one of said second plurality of data units.

14. (Original) The receiving mechanism of claim 13, wherein said first receiver comprises a first delay control mechanism for adjusting said first variable delay, and wherein said second receiver comprises a second delay control mechanism for adjusting said second variable delay.

15. (Original) The receiving mechanism of claim 14, wherein said first delay control mechanism adjusts said first variable delay to cause said first receiver to generate said first plurality of latching control signals such that each of said first plurality of latching control signals coincides more closely with a midpoint of a data period corresponding to one of said first plurality of data units.

16. (Original) The receiving mechanism of claim 15, wherein said second delay control mechanism adjusts said second variable delay to cause said second receiver to generate said second plurality of latching control signals such that each of said second plurality of latching control signals coincides more closely with a midpoint of a data period corresponding to one of said second plurality of data units.

17. (Original) The receiving mechanism of claim 16, wherein said first delay control mechanism adjusts said first variable delay to cause said first reference signal to coincide more closely with a midpoint of a data period corresponding to one of said first plurality of data units.

18. (Original) The receiving mechanism of claim 17, wherein said second delay control mechanism adjusts said second variable delay to cause said second reference signal to coincide more closely with a midpoint of a data period corresponding to one of said second plurality of data units.

19. (Original) The receiving mechanism of claim 16, wherein said first delay control mechanism comprises:

a detection mechanism, said detection mechanism receiving an indication of how closely each of said first plurality of latching control signals coincides with a midpoint of a data period corresponding to one of said first plurality of data units, and providing an adjustment signal to adjust said first variable delay.

20. (Original) The receiving mechanism of claim 19, wherein said detection mechanism comprises a phase detector.

21. (Original) The receiving mechanism of claim 19, wherein said first delay control mechanism further comprises:

a fixed delay element coupled to receive at least one of said first plurality of latching control signals and providing a delayed latching signal; and

a latching component coupled to receive said first data stream, said latching component latching one of said first plurality of data units in response to said delayed latching signal.

22. (Currently amended) ~~The~~ A multi-link receiving mechanism ~~of claim 21,~~ comprising:

a first receiver coupled to receive a first data stream and a clock signal, said first data stream comprising a first plurality of data units, said first receiver delaying said clock signal by a first variable delay to derive a first reference signal, and generating a first plurality of latching control signals based upon said first reference signal to latch said first plurality of data units; and

a second receiver coupled to receive a second data stream and said clock signal, said second data stream comprising a second plurality of data units, said second receiver delaying said clock signal by a second variable delay to derive a second reference signal, and generating a second plurality of latching control signals based upon said second reference signal to latch said second plurality of data units;

wherein said first data stream and said second data stream are not aligned with each other when received by said first receiver and second receiver, respectively;

wherein said clock signal is not necessarily aligned with either said first data stream or said second data stream;

wherein each of said first plurality of data units occupies one data period, and wherein said first receiver generates no more than one of said first plurality of latching control signals per data period;

wherein each of said first plurality of latching control signals coincides approximately with a midpoint of a data period corresponding to one of said first plurality of data units;

wherein each of said second plurality of data units occupies one data period, and wherein said second receiver generates no more than one of said second plurality of latching control signals per data period;

wherein each of said second plurality of latching control signals coincides approximately with a midpoint of a data period corresponding to one of said second plurality of data units;

wherein said first receiver comprises a first delay control mechanism for adjusting said first variable delay, and wherein said second receiver comprises a second delay control mechanism for adjusting said second variable delay;

wherein said first delay control mechanism adjusts said first variable delay to cause said first receiver to generate said first plurality of latching control signals such that each of said first plurality of latching control signals coincides more closely with a midpoint of a data period corresponding to one of said first plurality of data units;

A1

wherein said second delay control mechanism adjusts said second variable delay to cause said second receiver to generate said second plurality of latching control signals such that each of said second plurality of latching control signals coincides more closely with a midpoint of a data period corresponding to one of said second plurality of data units;

wherein said first delay control mechanism includes a detection mechanism to receive an indication of how closely each of said first plurality of latching control signals coincides with a midpoint of a data period corresponding to one of said first plurality of data units and to provide an adjustment signal to adjust said first variable delay;

wherein said detection mechanism comprises a phase detector;

wherein said first delay control mechanism further comprises:

a fixed delay element coupled to receive at least one of said first plurality of latching control signals and providing a delayed latching signal; and

a latching component coupled to receive said first data stream, said latching component latching one of said first plurality of data units in response to said delayed latching signal; and

wherein said detection mechanism receives said one of said first plurality of data units, and compares said one data unit with a plurality of other data units from said first plurality of data units to determine how closely each of said first plurality of latching control signals coincides with a midpoint of a data period corresponding to one of said first plurality of data units.

23. (Original) The receiving mechanism of claim 22, wherein said fixed delay element has a fixed delay greater than one data period.

24. (Original) The receiving mechanism of claim 23, wherein said fixed delay is approximately (X + .5) times said data period where X is an integer greater than or equal to 1.

25. (Original) The receiving mechanism of claim 3, wherein said first receiver comprises a first delay locked loop coupled to receive said first reference signal, said first delay locked loop generating said first plurality of latching control signals based upon said first reference signal, and wherein said second receiver comprises a second delay locked loop coupled to receive said second reference signal, said second delay locked loop generating said second plurality of latching control signals based upon said second reference signal.

26. (Original) The receiving mechanism of claim 25, wherein each of said first plurality of data units occupies one data period, wherein said first delay locked loop generates no more than one of said first plurality of latching control signals per data period, and wherein each of said first plurality of latching control signals coincides approximately with a midpoint of a data period corresponding to one of said first plurality of data units.

27. (Original) The receiving mechanism of claim 26, wherein said first reference signal coincides approximately with a midpoint of a data period corresponding to one of said first plurality of data units.

28. (Original) The receiving mechanism of claim 27, wherein each of said second plurality of data units occupies one data period, wherein said second delay locked loop generates no more than one of said second plurality of latching control signals per data period, and wherein each of said second plurality of latching control signals coincides approximately with a midpoint of a data period corresponding to one of said second plurality of data units.

29. (Original) The receiving mechanism of claim 28, wherein said second reference signal coincides approximately with a midpoint of a data period corresponding to one of said second plurality of data units.

30. (New) A multi-link apparatus, comprising:

a first receiver to receive a first data stream; and

a second receiver to receive a second data stream in parallel with the first receiver receiving the first data stream;

a first delay to generate a first reference signal responsive to a clock;

a second delay to generate a second reference signal responsive to the clock;

a first signal generator to generate a plurality of first latching signals responsive to the first reference signal; and

a second signal generator to generate a plurality of second latching signals responsive to the second reference signal;

a first latching mechanism to latch the first data stream with the plurality of first latching signals; and

a second latching mechanism to latch the second data stream with the plurality of second latching signals.